ARMY RESEARCH LABORATORY

Gallium Arsenide (GaAs) Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication (ARL Tile #2)

by John Penn

ARL-TN-0404 **September 2010**

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Army Research Laboratory
Adelphi, MD 20783-1197

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14. ABSTRACT
High-performance microwave and radio frequency integrated circuits are of interest to the Army. Several monolithic microwave integrated circuits (MMICs) were designed to enhance the performance of commercial-off-the-shelf (COTS) RF integrated circuits (RFICs) used in many wireless systems. This report is a summary of the steps and documentation delivered to TriQuint for their Prototype Development Quickturn (PDQ) Option for a set of MMIC designs fabricated for the U.S. Army Research Laboratory (ARL). This is an optimized set of designs based on some previous work. In this design submission, there are 10 separate MMIC designs on the 5 x 10 mm quarter tile.

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1. Introduction

High-performance microwave and radio frequency integrated circuits are of interest to the Army. The ability to design custom integrated circuits and fabricate prototypes in a timely and cost-effective manner is a prime concern. Several monolithic microwave integrated circuits (MMICs) were designed to enhance the performance of commercial-off-the-shelf (COTS) RF integrated circuits (RFICs). One company that has various MMIC fabrication processes and prototype options for high-performance gallium arsenide (GaAs) semiconductors is TriQuint Semiconductor, Inc. This report is a summary of the steps and documentation delivered to TriQuint for their Prototype Development Quickturn (PDQ) Option for a set of MMIC designs fabricated for a U.S. Army Research Laboratory (ARL) time-to-live (TTL) program.

In the PDQ option, the customer gets a 5 x 10 mm quarter tile and shares the mask cost of prototyping one or two 6-in GaAs wafers. The cost of the PDQ option is about 1/3 of a full mask prototype, where one would get the entire tile for one or two 6-in GaAs wafers. This is an optimized set of designs based on some previous work along with some new enhancements. These designs focus on optimizing operation, predominantly centered around 425 MHz rather than the previous operation centered at 450 MHz. In this design submission, there are 10 separate MMIC designs on the 5 x 10 mm quarter tile.

2. Layout of the Tile

The design and simulation of the MMIC designs will be documented separately; this report is intended just to document the design submission process. Each design was initially simulated and a preliminary layout performed with Agilent's Advanced Design System (ADS) or Applied Wave Research's Microwave Office (MWO) software. The preliminary layouts were then arranged in a tile pattern such that the scribe or "cut" lines in the *x* and *y* directions were contiguous. Within limits, one can have differing die sizes, but every single row and column must have the same dimension and follow the guidelines of the foundry process. For this quarter tile design, 10 MMICs were laid out in two columns of 2410 µm width with three rows of 2410 µm height and two rows of 1270 µm height. ICED software was used to layout the tile and perform design verification including design rule checking (DRC) and layout versus schematic (LVS) checking. Figure 1 displays a plot of the tile layout, showing the arrangement of the 10 different designs. All of the MMIC designs were designed for a 95 x 95 mil or 95 x 50 mil die size to fit within a 4 x 4 mm quad no lead (QFN) flat pack package. A wirebond diagram of each layout was created in a 4 x 4 mm QFN package before submitting the layouts to fabrication.

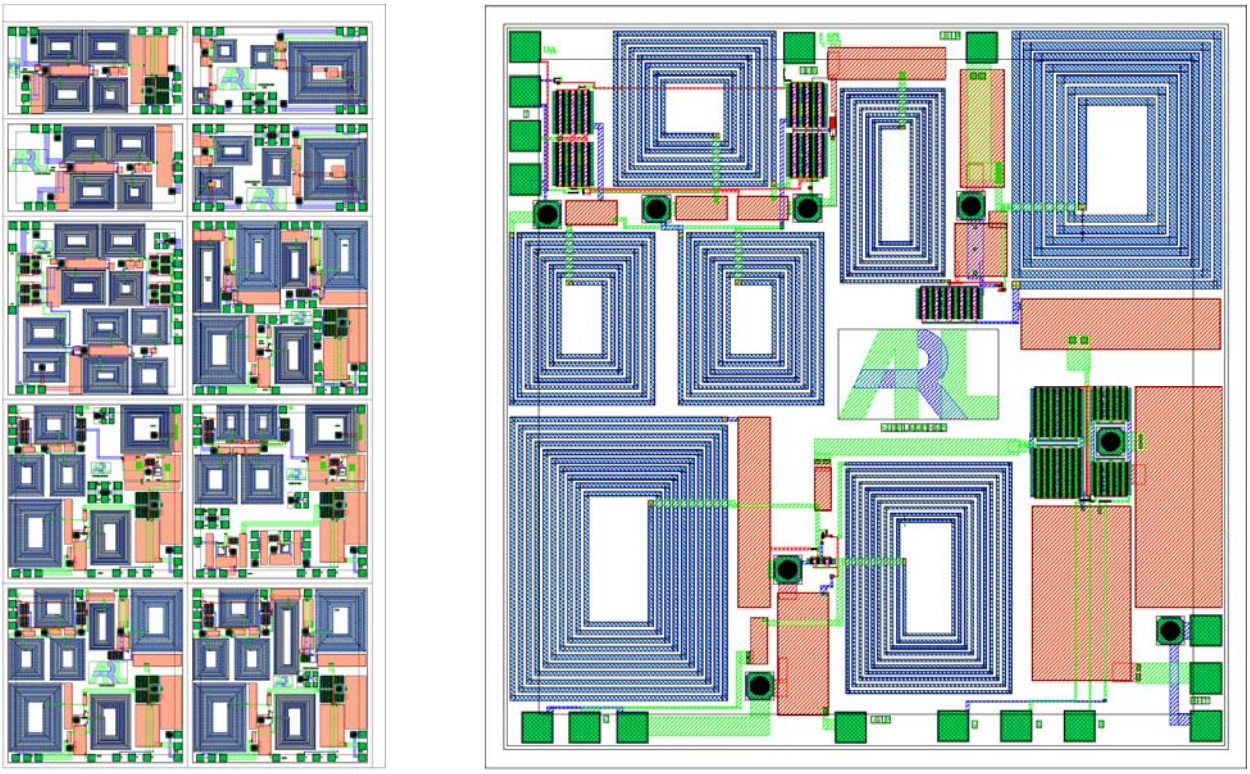

Figure 1. Plot of the 5 x 10 mm GaAs Tile #2 (left) and a typical 95 x 95mil design (right).

3. Summary of Designs

Every design in the tile must have a unique name less than 13 letters that is included on each die layout using appropriately sized text in first-level metal. A special pointer to the identifier text on each die is required by TriQuint to sort the die into individual packages. All designs were named in the format ARLNNFFFF, where "ARL" designates U.S. Army Research Laboratory, NN is a number for the design from 21 to 29, and FFFF designates the design frequency as M425 for 425 MHz, M900 for 900 MHz, and DB for dual band. There are two other exceptions in the naming. The first pass ARL tile used numbers of 01 to 15, so this second pass design uses numbers starting with 20, i.e., 21 to 29. ARL25 is a test chip for individual probe testing of several critical circuits. ARL29M900 and ARL29M900S are almost identical except that the S version has a single pole double throw switch to steer the RF output to one of two pads versus the initial design, which has a single RF output (antenna). Half of the designs are active RF front-end designs and half of the designs are matching circuits to integrate the numerous discrete lumped elements required by the RFIC transceiver into a single small package. The following is a brief summary of the 10 designs:

- ARL21M425–This 425-MHz design contains a binary phase shift key (BPSK) modulator, a 100-mW power amplifier (PA) for 2.8 V, a narrowband low DC power consumption low noise amplifier (LNA), and a transmit/receive switch (TRS) using positive voltage control inputs with negative threshold depletion pseudomorphic high electron mobility transistors (PHEMTs). It is a 95 x 95 mil die.
- ARL22M425–This 425-MHz design contains a BPSK modulator, a 50-mW PA for 2.8 V, a narrowband low DC power consumption LNA, and a TRS using positive voltage control inputs with negative threshold depletion PHEMTs. It is 95x95 mil die.
- ARL23M425–This 425-MHz design contains a BPSK modulator, a 50/75-mW PA for 2.8/3.6 V, a narrowband low DC power consumption LNA, and a TRS using positive voltage control inputs with negative threshold depletion PHEMTs. This design is intended to operate over a broader range of battery voltages. It is a 95x95 mil die.
- ARL24DB–This dual-band design contains a BPSK modulator for 425 or 900 MHz, the broadband 50/75-mW PA for 2.8/3.6 V, a broadband moderate DC power consumption LNA, and a TRS using positive voltage control inputs with negative threshold depletion PHEMTs. This design is intended to operate at either the 425 or 900 MHz frequency bands. It is a 95x95 mil die.
- ARL25–This is a test circuit of the individual designs in the previous four design variations. It contains a 100-mW PA for 2.8 V, a 50-mW PA for 2.8 V, a narrowband low DC power consumption LNA, and a TRS. It is a 95x95 mil die.
- ARL26DB–This dual-band design contains a matching circuit plus RF switches to connect the integrated matching circuit for a Texas Instruments (TI) cc1100 RFIC for operation at either 425 or 900 MHz. One side of the design connects to the differential RF connections of the cc1100 RFIC and the other side switches to one of two single ended RF connections, intended to be either an input to a transmitter/PA and the other an output from a receiver/LNA. It is a 95x95 mil die.
- ARL27M425–This design contains discrete lumped elements circuits for an integrated match at 425-MHz circuit for a TI cc1000 RFIC. It separates the recommended matching circuit into an RF input and RF output match for separate connections to either an input to a transmitter/PA and the other an output from a receiver/LNA rather than a single-ended connection to an antenna. It is a 95x50 mil die.
- ARL28M900–This design contains discrete lumped elements circuits for an integrated match at 900-MHz circuit for a TI cc1000 RFIC. It separates the recommended matching circuit into an RF input and RF output match for separate connections to either an input to a transmitter/PA and the other an output from a receiver/LNA rather than a single-ended connection to an antenna. It is similar to ARL27M425 except for the frequency of operation. It is a 95x50 mil die.

- ARL29M425–This single-band design contains a matching circuit to connect the integrated matching circuit for a TI cc1100 RFIC for operation at 425 MHz. One side of the design connects to the differential RF connections of the cc1100 RFIC and the other side connects to a single ended RF connection, intended to be the antenna connection. It is a 95x50 mil die.
- ARL29M425S–This single-band design contains a matching circuit to connect the integrated matching circuit for a TI cc1100 RFIC for operation at 425 MHz. One side of the design connects to the differential RF connections of the cc1100 RFIC and the other side connects to RF switches intended for connection to the input of a transmitter/PA or an output from a receiver/LNA rather than the single-ended connection to an antenna of ARL29M425, which is a similar design. It is a 95x50 mil die.

4. Design Rule Checking (DRC)

All designs within the tile must be checked according to the process design rules supplied by TriQuint. TriQuint has design rules for their fabrication processes that work with the open-source ICED program. Design verification typically consists of DRC and LVS checking. For fabrication feasibility, TriQuint only cares that the tile passes DRC checks and can be fabricated. While some design rules may be oriented towards maximizing yield and are not fatal errors, any violations of the design rules must be removed or granted a waiver to be fabricated by the foundry. Additionally, it is up to the designer to verify that the designs are connected as desired and that parameter values are correct by doing additional LVS checking.

After completing DRCs with ICED, a final DRC check was performed on the tile layout using TriQuint's "maildrc" service. TriQuint provides a free e-mail based service to provide a final DRC using Cadence's Assura software.

Next, there is a checklist for the foundry (see the appendix for details) to verify higher-level issues such as labeling. Each individual die must have a unique label using the correct metal layer and be of sufficient size. Every die name starts with the letters "ARL" to help identify the customer so that the individual dies can be sorted and returned appropriately.

5. Layout Versus Schematic Checking (LVS)

Each design is verified against a schematic (i.e., a netlist), which can be generated from MWO or ADS. Both tools require manual editing of the generated netlist, which typically requires an iterative LVS check until all device connections are verified. Foundries do not require LVS checking, only DRC, but it is imperative for the designer to verify the connections in the layout.

A DRC-correct layout does not guarantee that there are no shorts or missing connections that could cause the circuit to fail. Verifying the connections requires LVS checking followed by a final DRC if any layout changes occur. If the design passes DRC and LVS checking, then the probability of functional success is extremely high. In addition to checking the connections, the LVS check also notes parametric differences between the schematic and layout. If the capacitors, resistors, or PHEMTs differ in size, type, or value, the LVS check will list the mismatches. Inductors are not checked parametrically, only their connectivity is verified.

The MWO software has an excellent interface to the ICED software for DRC and LVS checking but still requires some manual editing of the netlist, while netlists generated by ADS generally require even more editing. One limitation in the LVS checking is that parameter values that use variable names rather than fixed values require manual editing of the netlist. Another limitation is that the simulators do not differentiate between individual via connections to ground, but the netlist checker does. The number of vias and their physical connectivity must match in the netlist and layout because LVS does not recognize the common ground connection of the substrate via. So, LVS could indicate a mismatch regarding ground vias that would not affect the actual performance of the circuit. It is possible to label ground vias and pads to help identify the actual errors/discrepancies in LVS that can be difficult to isolate.

Completing DRC and LVS checks should ensure a high probability of design success. There is still a possibility of amplifier stability issues that could require a second pass due to aggressive design, un-simulated coupling, or process variation. An electromagnetic (EM) simulator, such as Sonnet, can be used with the physical layouts to minimize errors due to unexpected or un-simulated coupling using MWO or ADS. Several of the circuits were simulated with Sonnet to verify the layouts and look for any unintended and unsimulated parasitics.

Since ICED is free open source software, it cannot be loaded on the computers connected to the Internet, which were used for simulation and layout using ADS and MWO. Transferring netlist files, etc., between a lab computer with ICED and the network computer containing the original simulation files and layouts could lead to some potential mismatches and errors in the design and verification process.

6. Design Data Sheet

TriQuint's customer design data sheet must be completed and submitted along with the standard Graphic Design System II (GDSII) layout file. Information is provided listing the unique die names of each design so that they can be sorted into individual gel packs. The design checklist is completed to ensure that the tile design has passed DRC checks and avoided common pitfalls. Any fabrication options are designated, such as 4-mil thinned wafers with substrate vias for this

design. Lastly, a plot of the tile layout is included. This plot should match what TriQuint sees when they import the GDSII file into their system.

7. PDQ Fabrication

TriQuint currently offers TQPED 0.5-um GaAs Enhancement/Depletion PHEMT prototype fabrication on a monthly basis. Actual fabrication time is about six weeks with substrate vias being the final step in the process; the via option adds an additional week to the schedule. For our ARL 24 August 2010 submission, the designs should be completion in early October 2010.

Probe testing of the designs will be documented separately as a technical note. This is intended to document the design submission steps for TriQuint's PDQ process and the customer data sheet that was provided for ARL's 24 August 2010 GaAs MMIC designs.

8. Attachment

The appendix includes a copy of the ARL PDQ customer data sheet for 24 August 2010.

9. References

Penn, J. E. *GaAs Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication*; ARL-TN-0381; U.S. Army Research Laboratory: Adelphi, MD, December 2009.

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Appendix. ARL PDQ Customer Data Sheet for 24 August 2010

The following is a copy of the ARL PDQ customer data sheet for 24 August 2010.

For TQO use only:
Mask Number_____

TRIQUINT OREGON PDQ CUSTOMER DATA SHEET

This data sheet, along with a symbolic quadrant representation, die list, and design file database are required to initiate a factory order at TriQuint. Mask plates will not be ordered without a fully completed and signed data sheet. Review the Foundry Handbook and complete the checklist on the last page before sending your data. Check the web-site http://www.tqs.com/extranet/foundry/application_notes.cfm for updated forms and current handbook. Note: Changes to a CDS form after submission, will require a new completed form to be submitted.

Send:

1) **Final GDSII Streamfile (database)**
2) **Customer Data Sheet**
3) **Die List**
4) **Symbolic Quadrant Representation**

To: foundry@tqs.com

Customer Name:	ARL_Adelphi_Lab	Date:	8/06/10
Primary Technical Contact:	John E. Penn	Phone #	301 394 0423
E-mail:	John.Penn4@us.army.mil	Alt. Phone #:	Enter Number
Secondary Contact:	Romeo Del Rosario	Phone #:	301 394 3562
E-mail:	romeo@arl.army.mil		
TQS Contact	Lisa Howard		
PO Number:	XXXX		

File Information

Indicate Clean Tape Deadline (as published on the web-site) that this tape is intended for: 8/24/10

Quadrant dimensions: (saw street center to saw street center).
Must be in 10 um increments. PCM allocation not necessary

Maximum dimension 5mm X 10mm X = (4820) um Y = (9770) um
Minimum dimension for quad is approximately 30% less of maximum dimensions

Layout Database Information:

(Note: For details on constructing the tile, refer to the Foundry Handbook)
GDS II Stream File name: arltile2
Top Level Cell Name: arltile2
Layout system used: ICED
DRC's used: : ICED TQPED V2.26
Design kit used (ex.ADS TQTRx_321) AWR_TQPED_v1.1.21_and ADS_TQPED_v2.34

LDR VERFICATION:

If data is not DRC clean or waivers not completed by due date, participation in PDQ may be delayed until next scheduled PDQ!

☒ YES ☐ NO Does this Stream File conform to the latest Layout Design Rules (LDR)? If NO please attach error list to this sheet
Any intentional design violations must be pre-approved by TQS and documentated.
** Approval needed for each submission, prior approvals do not carry forward**

☒ YES ☐ NO If TriQuint to perform DRC services, data needs to be submitted 2 weeks prior to scheduled data due date.

(Continued on Page 2)

Process Requirements: (Click box to select)

1. Choose one process 2. Choose SVIA or NO SVIA'S when not used in design.	
1.PROCESS	**2. SVIA**
☐ TQTRx	
☐ TQHBT3	
☐ TQRLC	☒ SVIA'S
☐ TQP13-N	☐ NO SVIA'S
☒ TQPED	
☐ TQBiHEMT	
☐ Other - Specify	

Thickness in mils: Note: All svia wafers are thinned to 4mils and includes backmetalization

☒ 4 (100um) ☐ 7 (175um) ☐ 10 (250um) ☐ No Thinning

Shipping Information:

To protect intellectual property, PDQs are shipped in either gel paks or on saw frames by die type.

Tape frames are an option only if 25 or less unique die types are present in quadrant, more than 25 will default to gel paks.

Shipping method: ☒ In gel paks by die type (default): Gel Pak; Vacuum Release™; Part #:***VR-103CC-00B-X4***

☐ On tape frames by die type (25 or less unique die type)

☐ Other- ***Use Special Instructions***

Special instructions:

** Approval for special instructions needed for each submission, prior approvals do not carry forward**

TQS PRE-APPROVAL REQUIRED (possible additional cost)

Enter Special Instructions Here

The person who fills out this form must type their name on the signed line. This counts as an electronic signature. TriQuint Foundry Services will provide mask making service based on information from this datasheet. Customer retains ownership of mask data. TriQuint maintains possession of the mask tooling. Customer signature releases data for mask creation and indicates that the customer has read and understood the Foundry Handbook.

Signed: John E. Penn Date: 8/06/10

Checklist:

The following is a check list of common problems that will result the rejection of the submitted data. **Most common errors causing data rejection are highlighted.** Review this list carefully to avoid these problems.

☒ Maximum quadrant size is 5 mm x 10 mm. Minimum size 30% less of the maximum quad

☒ All saw streets in the X and Y are continuous within the quad.

☒ Origin of quadrant is in lower left corner of saw street.

☒ No more than 14 saw streets in either the X or Y dimension.

☐ **Like die together and same size through out quad. If repeat die has different dimension, create unique label.**

☐ **Minimum of 2, maximum of 13 adjacent numeric or alpha characters for die labels, spaces count as a character. Any 12 character label must contain at least 1 dash (or underscore), and any 13 character label must have at least 2 dashes (or underscores)**

☒ All die labels in Metal 1. The only exception is TQP13 which uses sohmic(L39).

☒ **Die Label Marker pointing to all die. The Marker can be above, below, left, right or parallel but must be adjacent the die label and is the same scale. No features between the Marker and die label is permitted. Refer to Handbook for examples.**

☒ The minimum spacing between bond pads of adjacent die is 140 um.

☒ The final die size, and resulting quadrant size, must be in exact 10 um increment.

☒ All reference boundries on layer layer 60 (saw street centers) are continuous and coincident with adjacent die.

☒ The layout database maintains the minimum grid size indicated in the design manual.

☒ Structure names in GDS II stream file have no illegal Calma characters (i.e., dashes, asterisks, periods, etc.). Use only alpha-numeric characters. String length limited to 32 characters.

☒ **DRC is clean for all die in the quadrant. Any intentional design violations must be documentated and pre-approved by TQS**.

- Error of non-sortable Die Pad Sizes. ICED is mentioning HVR resistors below minimum length but it seems to be an extraneous error. There are a few narrow pads on a test cell repeated in a few of the designsl.

The Symbolic Quadrant Map and Die List:

For PDQs, TriQuint Oregon requires a symbolic quadrant map and a die list to be submitted along with data file.

The symbolic quadrant map is a representation of the quadrant layout referencing dimensions. die names and locations within the quadrant. Each die type is to be uniquely named. Die names must appear as they are labeled on the die. Include underscores, dashes, etc. if they are included in the label.

The die list contains contact information, die label and number of die per quadrant.

SAMPLE SYMBOLIC QUADRANT MAP AND DIE LIST:

Symbolic Quadrant for: (perfect_performance.gds)

Die Size		1010um	1010um	1070um	1070um	850um
		C1	C2	C3	C4	C5
2500um	R1	A12346	A12346	A54321	A54321	B123456
2500um	R2	A12346	A12346	A54321	A54321	B123456
2500um	R3	A12346	A12346	A54321	A54321	B123456
2500um	R4	A12346	A12346	A54321	A54321	B123456
2500um	R5	A12346	A12346	A54321	A54321	B54321
2500um	R6	A12346	A12346	A54321	A54321	B54321
2500um	R7	A12346	A12346	A54321	A54321	B54321
2500um	R8	A12346	A12346	A54321	A54321	B54321

(Remove unused rows and columns)

Die List:

	TQS Contact	Company Name / Designer	Die Label (met1)	die/ quad
1	Mr. Triquint Foundry	CIRCUITS-R-US Jeffry G.	A12346	16
2	Mr. Triquint Foundry	CIRCUITS-R-US Jeffry G.	A54321	16
3	Mr. Triquint Foundry	CIRCUITS-R-US Jeffry G.	B123456	4
4	Mr. Triquint Foundry	CIRCUITS-R-US Jeffry G.	B54321	4

Symbolic Quad Map for: (arltile2.sf) include row, column dimensions; add or delete rows, columns

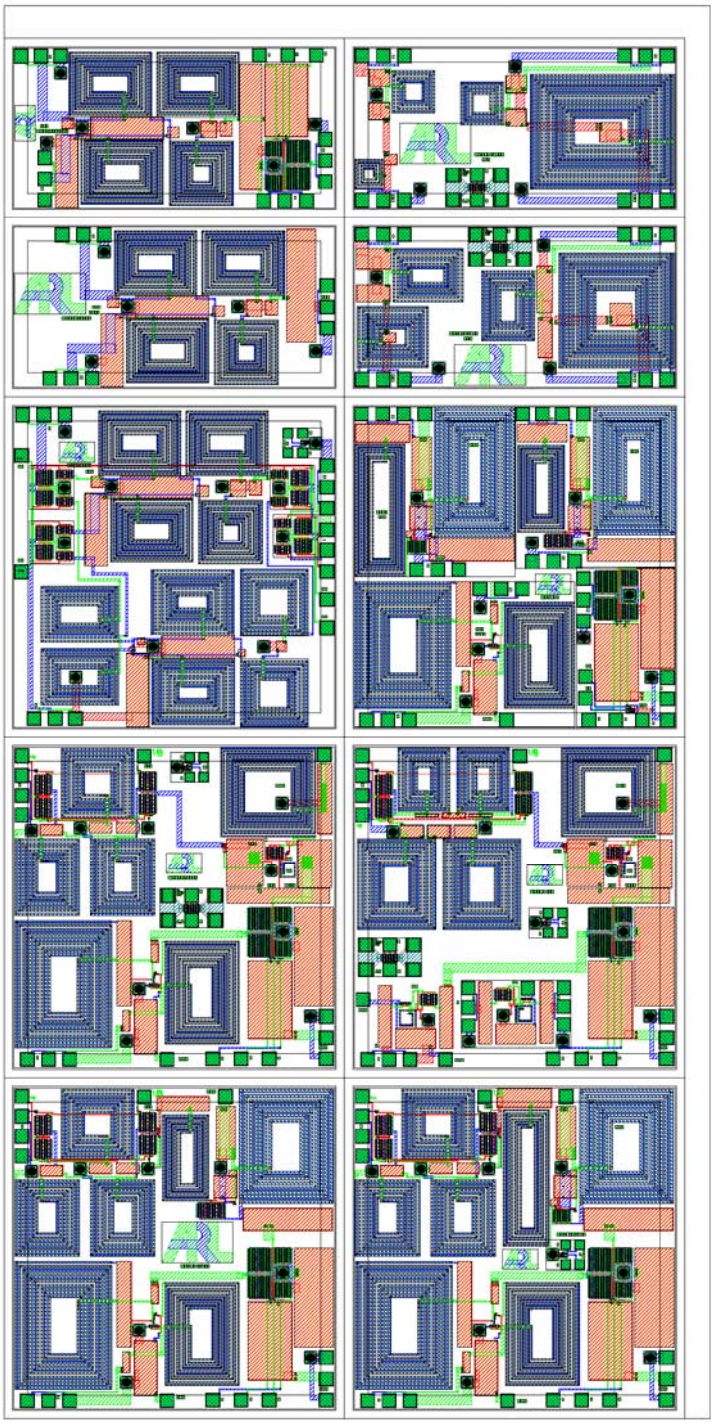
Die Size		2410um	2410um
		C1	C2
1270um	R1	ARL29M425S	ARL28M900
1270um	R2	ARL29M425	ARL27M425
2410um	R3	ARL26DB	ARL25
2410um	R4	ARL23M425	ARL24DB
2410um	R5	ARL21M425	ARL22M425

(Remove unused rows and columns)

Die List:

	TQS Contact	Company Name / Designer	Die Label (met1)	Die per Quad
1	Lisa Howard	ARL—John Penn	ARL21M425	1
2	Lisa Howard	ARL—John Penn	ARL22M425	1
3	Lisa Howard	ARL—John Penn	ARL23M425	1
4	Lisa Howard	ARL—John Penn	ARL24DB	1
5	Lisa Howard	ARL—John Penn	ARL25	1
6	Lisa Howard	ARL—John Penn	ARL26DB	1
7	Lisa Howard	ARL—John Penn	ARL27M425	1
8	Lisa Howard	ARL—John Penn	ARL28M900	1
9	Lisa Howard	ARL—John Penn	ARL29M425	1
10	Lisa Howard	ARL—John Penn	ARL29M425S	1

(Remove unused rows)



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List of Symbols, Abbreviations, and Acronyms

ADS	Advanced Design System
ARL	U.S. Army Research Laboratory
BPSK	binary phase shift key
COTS	commercial-off-the-shelf
DRC	design rule checking
EM	electromagnetic
GaAs	gallium arsenide
GDSII	Graphic Design System II
LNA	low noise amplifier
LVS	layout versus schematic
MMICs	monolithic microwave integrated circuits
MWO	Microwave Office
PA	power amplifier
PDQ	Prototype Development Quickturn
PHEMTs	pseudomorphic high electron mobility transistors
QFN	quad no lead
RFICs	RF integrated circuits
TI	Texas Instruments
TRS	transmit/receive switch
TTL	time-to-live

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